IN THE CLAIMS

Please amend the claims as follows:

1. (original) A processing system arranged for execution of a set of instructions under control of a program counter (PC), the processing system comprising:

- an execution unit (EX1, EX2);
- a first register file (RF1, RF2) for storing data, the first register file being accessible by the execution unit;
- a program memory (PM) for storing the set of instructions;
- a second register file (RF3) for storing a value of the program counter, the second register file being accessible by the execution unit (EX2),

and wherein the execution unit (EX2) is arranged to conditionally execute a dedicated instruction for writing a value of the program counter into the second register file.

2. (original) A processing system according to claim 1, wherein the processing system further comprises a controller (CTR); wherein the second register file is accessible by the controller; and wherein the controller is arranged to use the value of the program counter stored in the second register file, to fetch an instruction from the program memory.

3. (original) A processing system according to claim 2, wherein the controller is further arranged to increment the value of the program counter and to write the incremented value of the program counter into the second register file.

4. (original) A processing system according to claim 3, wherein the processing system is further arranged to write either the value of the program counter incremented by the controller into the second register file, or to write the value of the program counter produced by the execution unit into the second register file, depending on the evaluation of a branch condition.

5. (original) A processing system according to claim 1, characterized in that the execution unit (EX2) is further arranged to evaluate a branch condition and subsequently use the result of the evaluation as a guard (GU2) to conditionally execute a first dedicated instruction for writing a value of the program counter into the second register file.

6. (original) A processing system according to claim 1, characterized in that the execution unit (EX2) is further arranged to execute a second dedicated instruction;

the second dedicated instruction having at least a first argument and a second argument, the second argument being a value of the program counter;

wherein the second dedicated instruction is arranged to write the value of the program counter into the second register file, depending on the value of the first argument.

7. (original) A processing system according to claim 1, wherein the processing system is further arranged to execute a plurality of said dedicated instructions in parallel, and wherein during the compilation step it is guaranteed that only one instruction of the plurality of dedicated instructions is conditionally executed.

8. (original) A processing system according to claim 1, characterized in that the processing system is a data-stationary Very Large Instruction Word (VLIW) processor, wherein the VLIW processor further comprises:

- a plurality of execution units (EX1, EX2);
- a communication device (CN) for coupling the execution units and the first register file.

9. (original) A processing system according to claim 1, characterized in that the processing system is a time-stationary

Very Large Instruction Word (VLIW) processor, wherein the VLIW processor further comprises:

- a plurality of execution units (EX1, EX2);
- a communication device (CN) for coupling the execution units and the first register file;

and wherein the VLIW processor is further arranged to dynamically control the transfer of result data from an execution unit of the plurality of execution units to the first register file and the second register file, based on control information derived from the set of instructions.

10. (currently amended) A VLIW processor according to claim 8~~or 9~~, characterized in that the register file is a distributed register file (RF1, RF2).

11. (currently amended) A VLIW processor according to claim 8~~or 9~~, characterized in that the communication device is a partially connected communication network (CN).

12. (original) A method for executing a set of instructions by a processing system, wherein the processing system comprises:

- an execution unit (EX1, EX2);

- a first register file (RF1, RF2) for storing data, wherein the first register file is accessible by the execution unit;
- a program memory (PM) for storing the set of instructions;
- a second register file (RF3) for storing the program counter, wherein the second register file is accessible by the execution unit,
- and wherein the method comprises the following steps:

executing a dedicated instruction for writing a value of the program counter into the second register file;

using the value of the program counter for fetching an instruction from the program memory;

executing said instruction.

13. (original) A compiler program product being arranged for implementing all steps of the method for programming a processing system according to claim 12, when said compiler program product is run on a computer system.